A portable readout system for

Micro-pattern Gas detectors and Scintillation detectors

**Abstract**:

A system of readout electronics used in both Micro-pattern Gas detectors and Scintillator detectors as well as its performance are introduced in this paper. The system is intended as a general purpose multi-channel readout solution for a wide range of detector types and detector complexities. A 32-channel charge sensitive ASIC VATA160 from IDEAS company is adopted in this method. With its features of high integration, low noise and large dynamic range, the system handles up to 128 electronic channels and each channel’s dynamic range is from -3pC to +13pC with a noise of better than 2.5fC and nonlinearity of better than 0.5%. As a portable system, it acquires the detector signals either from external trigger inputs or from a synchronized trigger generated by the system itself. The system transfers data to a PC host and gets controlled by PC via only one Universal Serial bus (USB).

**Key words:** VATA160, ASIC, readout system, USB, MPGD, Charge measurement

1. **Introduction**:

With the development of high energy physics (HEP) experiments, the micro-pattern gas detector (MPGD) and scintillation detector are widely used in particle detection physics and space astrophysics. As a high resolution particle tracking detector, the MPGDs has a variety of applications, especially for the Micro-megas [1] and Gas Electron Multipliers (GEMs) [2], which are becoming increasingly important. The MPGDs have been used in a large number of particle physics experiments such as T2k [3], COMPASS [4] and ALICE [5]. Thanks to the feature of high detecting efficiency and high dynamic range, scintillation detector is used in high energy physics like DAMPE [6] , AMS [7] and PAMELA [8], which have now reached maturity.

The widespread use of the MPGD and scintillation detector drive the development of corresponding readout electronics. It would be interesting to test these kinds of detectors with an electronic system as similar as possible to those used at the real physics experiments, so a front-end readout chip as those used in MPGDs and scintillation detectors should be used. VATA160, which was used in the Dark Matter Particle Explore (DAMPE), is a 32 charge sensitive channels and high dynamic range charge measurement readout ASIC with trigger designed by IDEADS (Norway).

An electronic system based on VATA160, which can acquire 128 channels of analogue measurement has been developed. The system can be used to research the performance of MPGDs such as GEM and Micro-megas as well as scintillation detectors like BGO Calorimeter (BGO) and Plastic Scintillation Detector (PSD). This system is compact and portable. Its total dissipation is lower than 2.5W, which means it can be supplied by only one USB bus connected to PC. This USB bus, which also bears the mission of transferring data to PC host and get controlling signal from PC, is the only one cable connected to the electronic system. The user controls the system with the PC software in communication with a Field Programmable Gate Array (FPGA) which interprets and executes the commands. Since the VATA160 has the ability of generating trigger signals from input charge, the external trigger input is not necessary to the system.

1. **Overview of VATA160**:

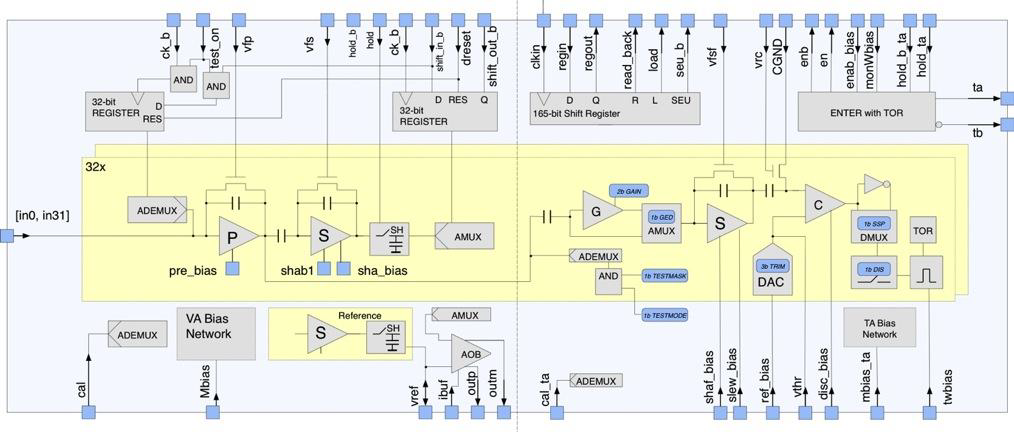


Figure 1 VATA160 internal architecture

VATA160 is a 32-channel, low noise (better than 2fC) and high dynamic range (-5pC to 13pC) charge measurement ASIC designed by IDEAS (Norway). Its internal architecture is shown in figure 1. VATA160 is combined by VA part and TA part. Each channel of VA part contains a charge sensitive preamplifier, a shaper circuit and a sample / hold circuit. An analog multiplexer controlled by the shift register is adopted to transfer the holding signals of 32 channels to the differential output port. Besides, there are calibration facilities for every channel to test its linearity. The TA part is in charge of generating fast trigger signals which can be used to drive the system to acquire sensor signals. Each channel consists of a shaper circuit and a comparator. An adjustable input reference voltage from outside is compared to the shaping amplitude produced by the shaper circuit. The TA part will output a trigger signal in the case that any of 32 channels’ shaping amplitude exceeds the reference voltage.

1. **Implement of readout system**:

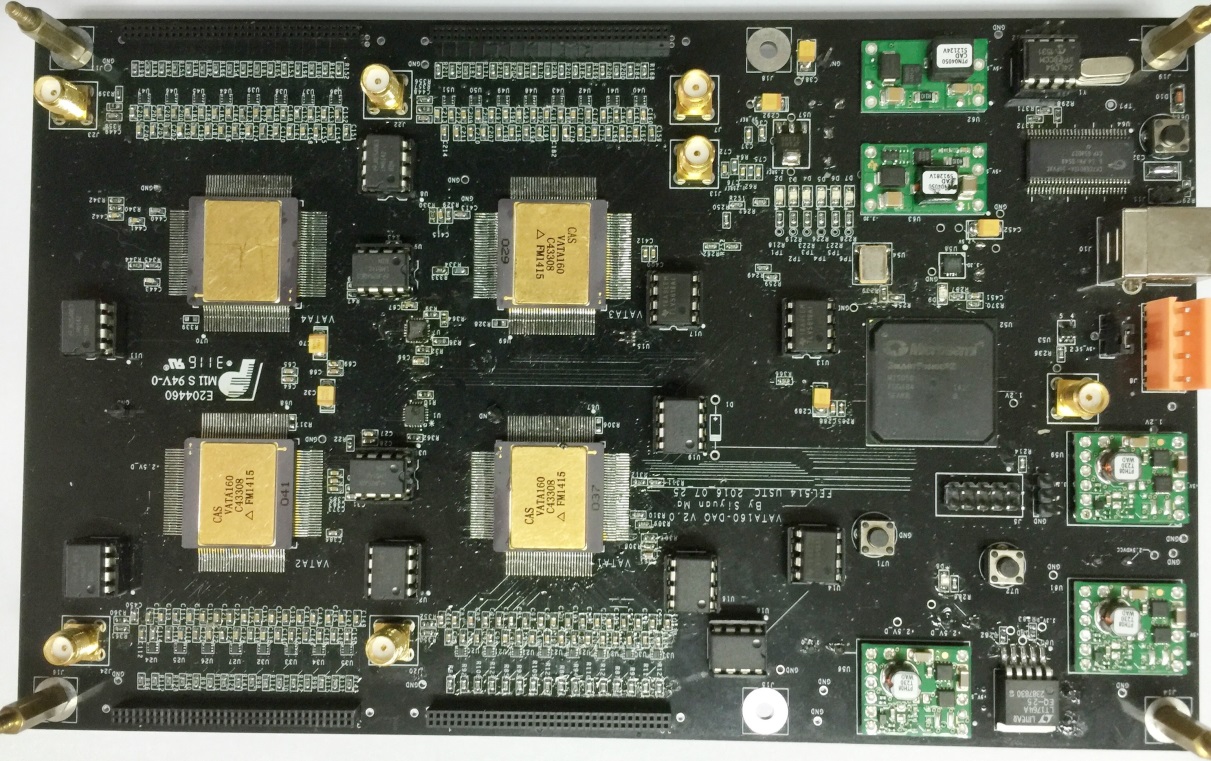


Figure 2 implement of the readout system

A portable readout system was designed and implemented based on the ASIC chip VATA160, whose dynamic range and noise were suitable for MPGD and scintillation detector. The system has two main parts: a hardware part and a software part (figure 2). The hardware part acquires the sensor signals either from a synchronized trigger output generated by the system itself, or from external trigger inputs. The data transfers to PC host through a USB cable, which is also responsible for power supply of hardware part and transmission of control commands from PC to hardware part.

* 1. **Hardware for readout system**



Figure 3 block diagram of electronic board

The block diagram of electronic board is given in figure 3. Its major parts will be introduced below.

* + 1. ESD protection of input signal



Figure 4 block diagram of the protecting circuit

In case of Electro-Static Discharge (ESD) and possible overvoltage “spark” from high voltage components in MPGD and scintillation detector, a clamping circuit is designed for protecting the ASIC chip VATA160. The diagram is shown in figure 4. The protecting circuit is composed of two diodes, a serial resistor and a serial capacitor. A micro-semi silicon diode array (NUP4114) is adapted. The ESD protecting level is for the IEC standards: IEC 61000-4-2 Level, which means a protection of a 16000V of human body model or 400V machine model [9].

* + 1. Charge measurement

Each signal of 128 channels going into VATA160 is integrated by charge sensitive pre-amplifier (CSA) and shaped into a semi-Gaussian pulse with the peak time of about 1.8 us. A hold signal from FPGA to VATA160 is used to sample all analog channels at the same time. When hold signal goes high, the analog switch in all sample-hold circuits will be turned off, and the 128 shaping amplifier outputs will be stored in their capacitors and wait for being sent out sequentially in the form of differential current, under the control of a chain of shifter registers and an analog multiplexer. Besides, a dummy channel inside each ASIC VATA160 is used as a reference for the output driver to reduce the common noise and temperature drifting.

The output currents of 4 VATA160s are respectively led to a current-to-voltage circuit formed by operational amplifiers, and digitized by an AD7944 chip, which is a 14-bit ADC with an input range from 0V to 5V. After digitizing, the data of 4ADCs are sent to FPGA to be packed and transferred to PC host via the USB cable.

* + 1. Trigger generation

The system is able to generate trigger signals itself to drive acquisition thanks to the TA part of VATA160 ASIC. The integrated pulse from the CSA of VA part will firstly be shaped into a fast narrow pulse in TA part and then discriminated by a comparator to generate a digital signal, which will be sent to the FPGA to be analyzed and generate a trigger signal. All the 32 outputs of TA part are internally OR’ed together.

* + 1. Calibration circuits

For the purpose of monitoring the performances of the system conveniently, a calibration circuit is designed, based on the calibration function of VATA160 ASICs.

The diagram of the calibration circuit, which is mainly composed of an analog switch and a 5k ohm resistor, is shown in Figure 5. The circuit will generate a step pulse from 0 to Vcal and a current pulse is injected into the ASIC chip through a 10pF capacitor. A digital to analog converter (DAC) and an op-amplifier are used to offer the calibration voltage Vcal. In the VA part of VATA160 chip, an analog de-multiplexer is used to determine which input channel is enabled for calibration. The scan curve of all 128 channels is acquired by selecting the input channels sequentially and increasing the calibration voltage gradually. The nonlinearity from -5pC to +10pC is less than 1%.



Figure 5 block diagram of the calibration circuit

不需要

Figure 6 calibration scan curve of a input channel

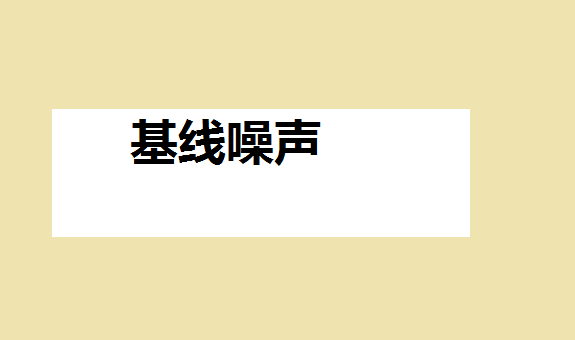
* 1. **Software for readout system**

The system is controlled by a Graphical User Interface (GUI) written in LabWindows and running on a windows PC, as shown in Figure 7. By setting the start-end voltage and step voltage, pedestal test and calibration test of all 128 channels can be performed automatically in 5 minutes. The configuration of the system is intelligent that the only thing you need to do in order to start acquisition is to choose trigger mode and set threshold.



Figure 7 diagram of software

1. **Performance of readout system**:

In this section, we present the results of performance test of the readout system. The electronic noise was firstly test and the result is shown in fig. 8. The fig indicates that the noise of every channel is better than 2.5fC.

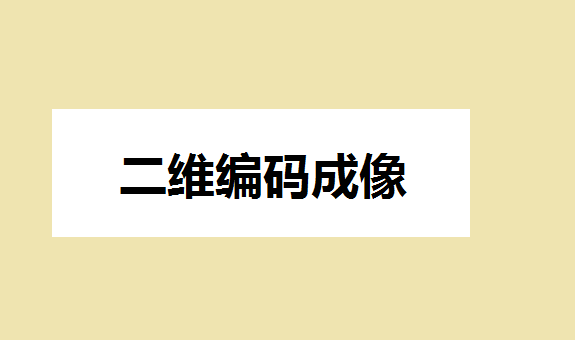


Due to the VATA160 chip having calibration circuits, the automatic calibration function was implemented on the system. A Digital-to-Analog converter (DAC, TLV5618) and an analog switch (ADG741) controlled by FPGA are used to generate step pulses with different amplitudes. There is a 10pF capacitor on the board between switch and VATA160 chip, through which the pulses is turned into a certain charge which covered the full range of the ASIC chip. Then the charge is injected into each channel of VATA160 chip one by one and the results are gotten and packaged by FPGA. As is shown in fig. 9, the typical results of integral nonlinearity (INL) between -3 to +13pC is better than 0.5%.

The system was coupled with a Micro-megas detector to test the energy spectrum of 55Fe. The result is shown in Fig. 10. The all-around peak and escape peak are clearly visible, which means the readout system is capable of performing the readout of Micro-megas detector.



The encoded multiplexing readout method for Thick Gas Electron Multiplier (THGEM) is a novel method which can significantly reduce the number of readout channels. [10] In this part, the readout system is connected to a THGEM detector with the Two-Dimensional direct coding readout of 100\*100 anode bar to perform imaging test. There is a copper plate with letter slits between the detector and X-ray generator. After collecting the X-ray signal, which enters the detector through the slit of the copper plate, the two-dimensional imaging is obtained by decoding the hit position of the incident signal. As is shown in Fig. 11, the letter gap is clearly visible when the threshold is chosen to triple the noise.



1. **Conclusion**:

A portable readout electronics system for MPGDs and Scintillation detectors are presented in this paper. It shows the readout systems has features of low noise (less than 2.5fC), high dynamic range (-5~+10pC), low power dissipation (less than 2.5W) and high integration (128 channels). The system is portable to use with only one USB bus for its supply, commands and data transmission. This system can operate with different types of MPGDs and Scintillation detectors.

**Refference**:

[1] Y. Giomataris, et al., Nucl. Instr. Meth. A, 376: 29-35 (1996).

[2] F. Sauli, Nucl. Instr. Meth. A, 386: 531-534 (1997).

[3] R. Tacik, The T2K fine-grained detectors, these proceedings

[4] Abbon P, Albrecht E, Alexakhin V Y, et al., Nucl. Instr. Meth. A, 577(3): 455-518 (2007).

[5] Lautridou P, Cussonneau J P, Ramillien V, et al., No. ALICE-INT-1997-28, (1997).

[6] Design of the Readout Electronics for the Qualification Model of DAMPE BGO Calorimeter

[7] Adloff C, Basara L, Bigongiari G, et al. The AMS-02 lead-scintillating fibres Electromagnetic Calorimeter[J]. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2013, 714: 147-154.

[8] O. ADRIANI, M. BOSCHERINI, G. CASTELLIN et al. IL NUOVO CIMENTO, 1999, VOL. 112 A, N.

11:1317‐1323

[9] datasheet of NUP4114

[10] A novel method of encoded…